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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application Serial No. 10/615,287
Confirmation No. 8293
Filing Date July 7, 2003
Inventor Kunal R. Parekh et al.
Assignee Micron Technology, Inc.
Group Art Unit 2812
Examiner Jey Tsai
Attorney Docket No. MI22-2260
Customer No. 021567
Title Methods of Forming Memory Circuitry

ATTENTION: KIM DUNCAN
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

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TRANSMITTAL FORM	Application Number	10/615,287	
	Filing Date	July 7, 2003	
	First Named Inventor	Kunal R. Parakh	
	Art Unit	2812	
	Examiner Name	H. Jay Tsai	
(to be used for all correspondence after initial filing)		Attorney Docket Number	MI22-2260
Total Number of Pages in This Submission			

ENCLOSURES (Check all that apply)		
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Wells St. John P.S.		
Signature			
Printed name	Mark S. Matkin		
Date	10/8/04	Reg. No.	32,268



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This collection of information is required by 37 CFR 1.6. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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 Micron Technology, Inc.

 Filed: 10/08/04

The stamp of the U.S. Patent and Trademark Office acknowledges receipt of the following papers relating to the Patent application of Kunah R. Parekh et al., Serial No. 10/615,287, filed 07/07/03, entitled "Methods of Forming Memory Circuitry"

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 10/615,287
 Filing Date July 7, 2003
 Inventor Kunal R. Parekh et al.
 Assignee Micron Technology, Inc.
 Group Art Unit 2812
 Examiner H. Jey Tsai
 Attorney Docket No. MI22-2260
 Customer No. 021567
 Title Methods of Forming Memory Circuitry

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States Code and that such willful false statement may jeopardize the validity of the application or any patent issued therefrom.

Dated at Spokane, Washington this 8th day of October, 2004.

Printed Name: Jim Tisack

(**EV372468649****IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Application Serial No. 10/615,287
Filing Date July 7, 2003
Confirmation No. 8293
Inventor Kunal R. Parekh et al.
Assignee Micron Technology, Inc.
Group Art Unit 2812
Examiner H. Jey Tsai
Attorney's Docket No. MI22-2260
Customer No. 021567
Title Methods of Forming Memory Circuitry

FILING TO CORRECT ERRONEOUS TRANSMITTAL FORM
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From: Mark S. Matkin (Tel. 509-624-4276; Fax 509-838-3424)
Wells St. John P.S.
601 West First Avenue, Suite 1300
Spokane, WA 99201-3828

REMARKS

This document is being filed merely to correct a clerical error in the filing of a previous Response to September 27, 2004, Final Office Action – Preliminary Amendment to Accompany RCE Filing, filed on October 4, 2004. A complete copy of the last-filed response, including the erroneous Transmittal Form, is included herewith along with proof of filing in the form of an Ex Post Declaration of Express Mailing and U.S. Express Mail. The Transmittal Form that

accompanied said previous response listed the wrong patent application information, and this filing corrects that clerical error by re-submitting the October 4, 2004 Response with the correct information listed on the Transmittal Form.

It is respectfully requested that the \$790 filing fee paid with the above-mentioned October 4, 2004 filing be credited to the RCE filing in this 10/615,287 application, if such has not been done so already.

Respectfully submitted,

Dated: 10-8-04

By: 

Mark S. Matkin
Reg. No. 32,268

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 10/615,287
 Filing Date July 7, 2003
 Inventor Kunal R. Parekh et al.
 Assignee Micron Technology, Inc.
 Group Art Unit 2812
 Examiner J. Hey Tsai
 Attorney Docket No. MI22-2260
 Customer No. 021567
 Title Methods of Forming Memory Circuitry

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Dated at Spokane, Washington this 4th day of October, 2004.

Rhonda G Rambo
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